AMENDMENTS TO THE CLAIMS

LISTING OF CLAIMS IN THE CASE

The following listing of Claims replaces all previous listings:

1. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Claim 2. (Previously Presented) A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal.

Claim 3. (Original) A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition

when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 6. (Previously Presented) A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 7. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor.

Claim 8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. (Original) A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. (Currently Amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a lowest level ~~provided by~~ the voltage regulator is specified to output.

Claim 12. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor

in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator comprising:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

the voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode;

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Claim 14. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;

a voltage source furnishing a value higher than the selectable voltage; and

a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

15. (Previously Presented) The circuit of Claim 14, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode.

16. (Previously Presented) The circuit of Claim 15, wherein the feedback circuit comprises a voltage divider.

17. (Previously Presented) The circuit of Claim 14, wherein the feedback circuit comprises a voltage divider.

18. (Previously Presented) The method of Claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator.

19. (New) A computer system comprising:

a processing unit;

circuitry coupled to the processor unit, said circuitry configured to provide to said processing unit:

a sleep voltage;

a first operating voltage; and

a second operating voltage that is less than the first operating voltage;

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

20. (New) A computer system as recited in Claim 19 wherein said allowed time is based on a configuration of said computer system.

21. (New) A computer system as recited in Claim 19 wherein said allowed time is based on timing requirements of said computer system.

22. (New) A computer system as recited in Claim 21, wherein said timing requirements are based on interrupt response times.

23. (New) A computer system as recited in Claim 19 wherein said first and second transition times are based on respective first and second voltage ramp times.

24. (New) A computer system as recited in Claim 19 wherein said sleep voltage is sufficient to maintain state of said processing unit but is not sufficient to maintain processing activity in said processing unit.

25. (New) A method of operating a computer processor, said method comprising:

transitioning from providing a sleep voltage to said computer processor to providing a first operating voltage to said computer processor within an allowed time for transitioning from a sleep state to an operating state; and

transitioning from said providing said first operating voltage to said computer processor to providing a second operating voltage to said computer processor, wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

26. (New) A method in accordance with Claim 25 wherein said second operating voltage is greater than said first operating voltage.

27. (New) A method in accordance with Claim 25 further comprising:

enabling a system clock to said computer processor when providing said first operating voltage to said computer processor; and

disabling said system clock to said computer processor when providing said sleep voltage to said computer processor.

28. (New) A method in accordance with Claim 25, wherein said sleep voltage is sufficient to maintain state of said computer processor but is not sufficient to maintain processing activity in said computer processor.

29. (New) A computer system comprising:

a processor;

an adjustable voltage supply configured to output to said processor:

a sleep voltage; and

a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable

from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

30. (New) A computer system as recited in Claim 29, wherein said adjustable voltage supply is further configured to output to said processor a second operating voltage that, based on a rate of transitioning from said sleep voltage to said second operating voltage, is achievable from said sleep voltage within said allowed time for transitioning from said sleep state to said operating state.

31. (New) A computer system as recited in Claim 29 wherein said allowed time is based on a configuration of said computer system.

32. (New) A computer system as recited in Claim 29 wherein said adjustable voltage supply comprises a voltage regulator.

33. (New) A computer system comprising:

a processing unit;

circuitry coupled to the processor unit, said circuitry configured to provide to said processing unit:

a first sleep voltage and a second sleep voltage;

a first operating voltage when transitioning from said first sleep voltage; and

a second operating voltage when transitioning from said second sleep voltage.

34. (New) A computer system as recited in Claim 33, wherein said circuitry is further configured to provide to said processing unit:

said first sleep voltage when transitioning from said first operating voltage; and

said second sleep voltage when transitioning from said second operating voltage.

35. (New) A computer system as recited in Claim 33 wherein a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

36. (New) A computer system as recited in Claim 33 wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage.

37. (New) A computer system as recited in Claim 36 wherein a voltage transition from said second sleep voltage to said first operating voltage is greater than a time allowed for transition from a sleep state to an operating state of said computer system.